

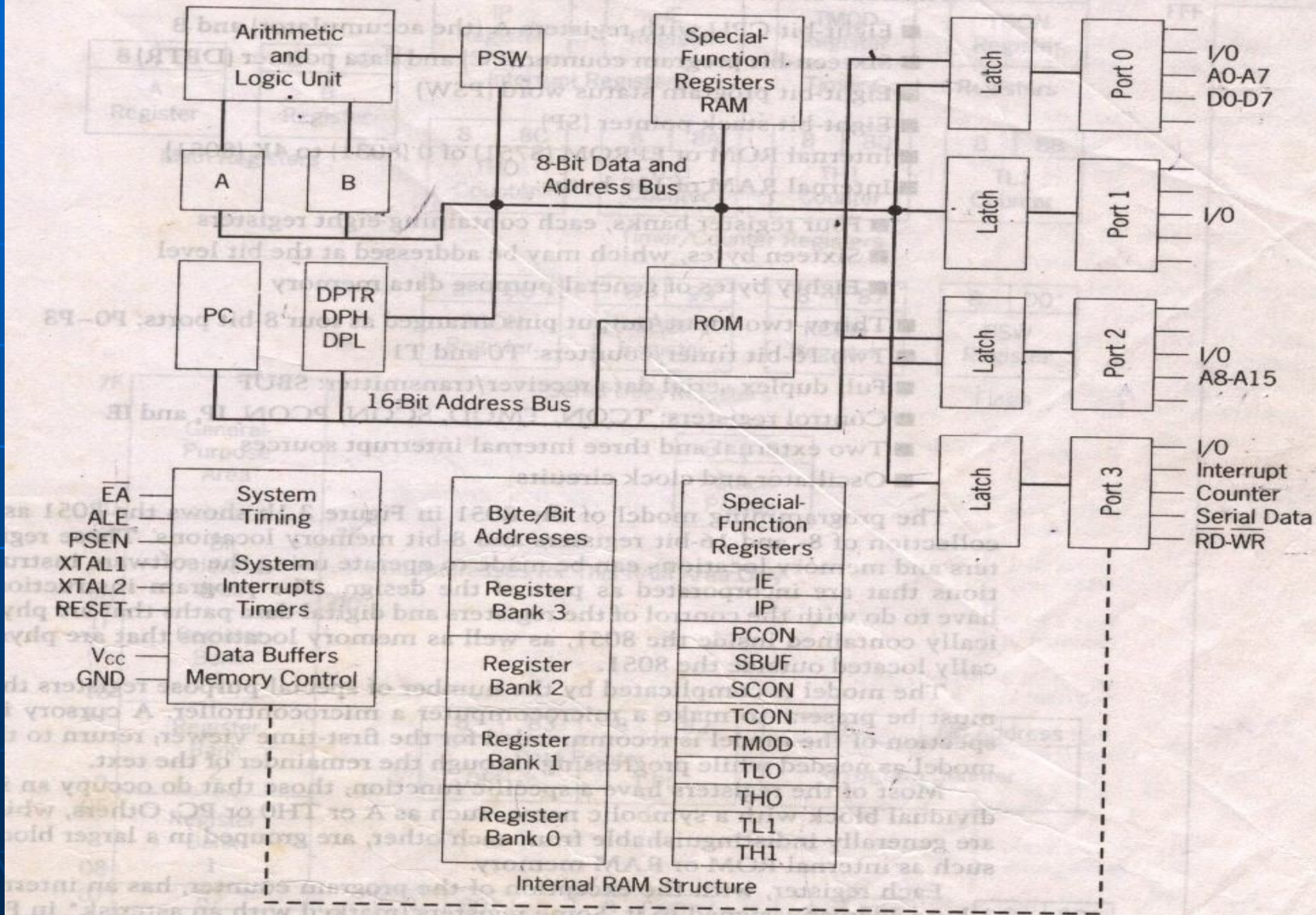
8051 Microcontroller

8051 Features

- 8 bit CPU with registers A and B
- 16 bit program counter (PC) and data pointer (DPTR)
- 8 bit program status word (PSW)
- 8 bit stack pointer
- Internal ROM of 0(8031) to 4K(8051)
- Internal RAM of 128 Bytes
 - 4 register banks 00-1f
 - 16bytes(bit addressable) 20-2f
 - 80 bytes of general purpose data memory 30-7f
- 32 I/O pins arranged as four 8 bit ports (P0± P3)
- 2 16-bit timer/counters: T0 and T1
- Full duplex serial data receiver/transmitter: SBUF
- Control registers: TCON, TMOD, SCON, PCON, IP and IE
- 2 external and 3 internal interrupt sources
- Oscillator and clock circuits

Block Diagram of 8051

Figure 3.1a 8051 Block Diagram



8051 Oscillator and Clock

- The oscillator is formed by the crystal, capacitors and an on-chip inverter.
- Circuitry that generates the clock pulses by which all internal operations are synchronized.
- Frequency- 1mHz to 16 mHz
- Minimum frequencies imply that some internal memories are dynamic and must always operate above a minimum frequency or data will be lost.
- The time to execute an instruction is found by
 - $T_{inst} = (C \times 12d) / \text{Crystal Frequency}$
 - Where C – number of machine cycles

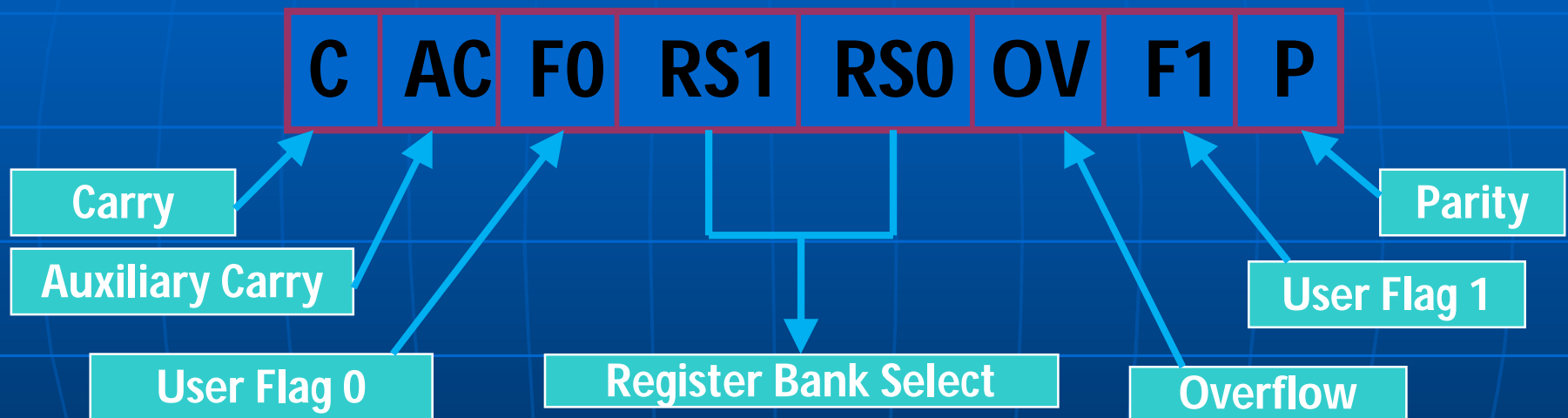
Program counter and Data Pointer

- PC does not have an internal address.
- Program instruction bytes are fetched from locations in memory that are addressed by the PC.
- DPTR register is made up of two 8 bit registers, named DPH and DPL, which are used to furnish memory addresses for internal and external code access and external data access.
- DPTR does not have a single internal address; DPH and DPL are each assigned an address.

A and B CPU register

- 8051 contains 34 general purpose or working registers.
- Two of these registers A and B, hold results of many instructions, particularly math and logical operations, of the CPU.
- Other 32 register are arranged as part of internal RAM in four banks.
- 'A' register:
 - Is most versatile of the two registers.
 - It is used for many operations (arithmetical, logical and bit manipulations).
 - Used for all data transfers between the 8051 and any external memory.
- 'B' register:
 - Used with A register for multiplication and division operations
 - No other function other than as a location where data may be stored.

Flags and Program Status Word [PSW]



Internal Memory

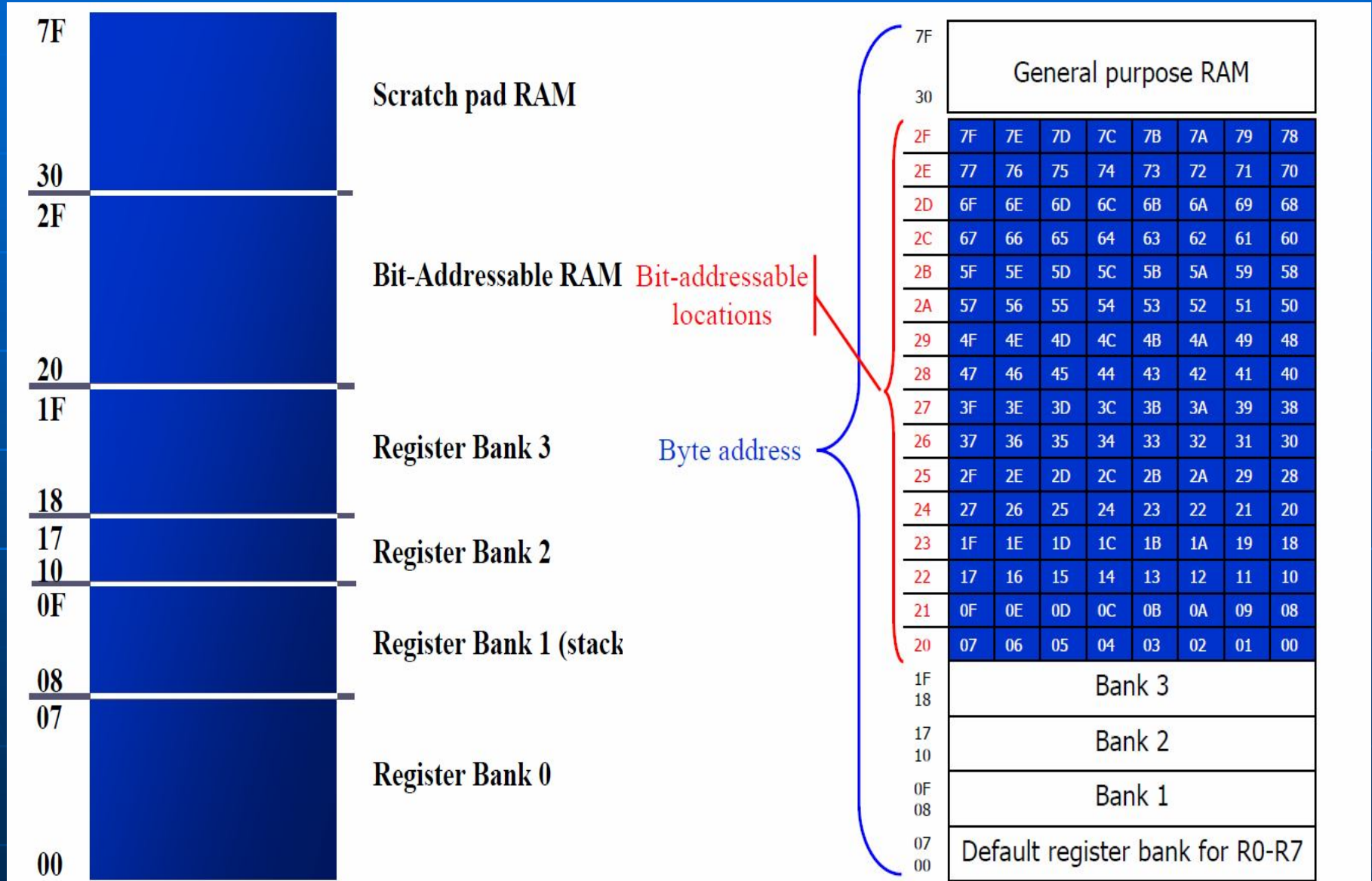
- Internal ROM
- Internal RAM

128 Byte RAM

- There are 128 bytes of RAM in the 8051.
 - Assigned addresses 00 to 7FH
- The **128 bytes** are divided into **3 different groups** as follows:
 1. A total of **32 bytes** from locations 00 to 1F hex are set aside for *register banks*.
 2. A total of **16 bytes** from locations 20H to 2FH are set aside for *bit-addressable* read/write memory.
 3. A total of **80 bytes** from locations 30H to 7FH are used for read and write storage, called *scratch pad*.



8051 RAM with addresses



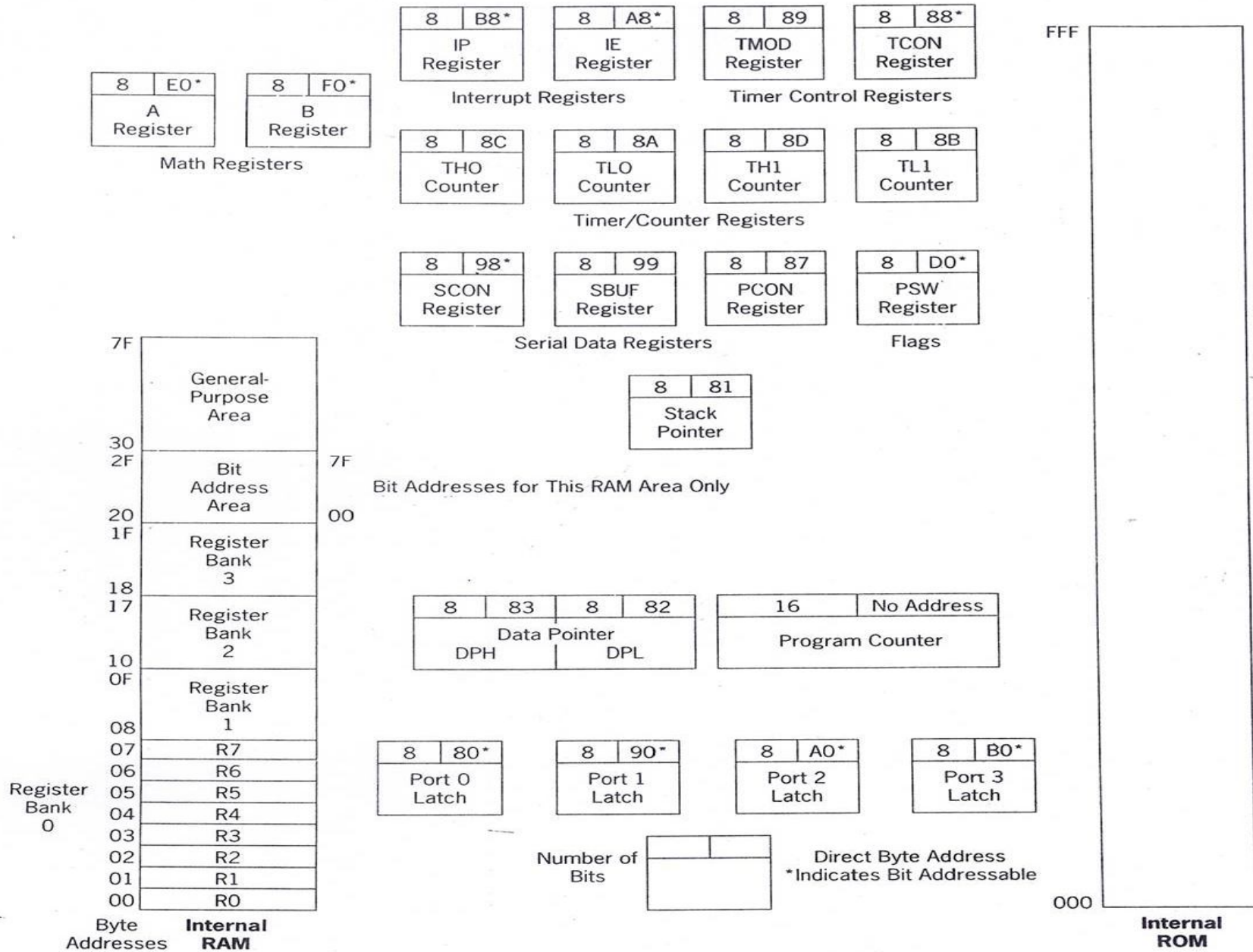
8051 Register Bank Structure



8051 Register Banks with address

Register bank 0		Register bank 1		Register bank 2		Register bank 3	
00	R0	08	R0	10	R0	18	R0
01	R1	09	R1	11	R1	19	R1
02	R2	0A	R2	12	R2	1A	R2
03	R3	0B	R3	13	R3	1B	R3
04	R4	0C	R4	14	R4	1C	R4
05	R5	0D	R5	15	R5	1D	R5
06	R6	0E	R6	16	R6	1E	R6
07	R7	0F	R7	17	R7	1F	R7

Figure 3.1b 8051 Programming Model



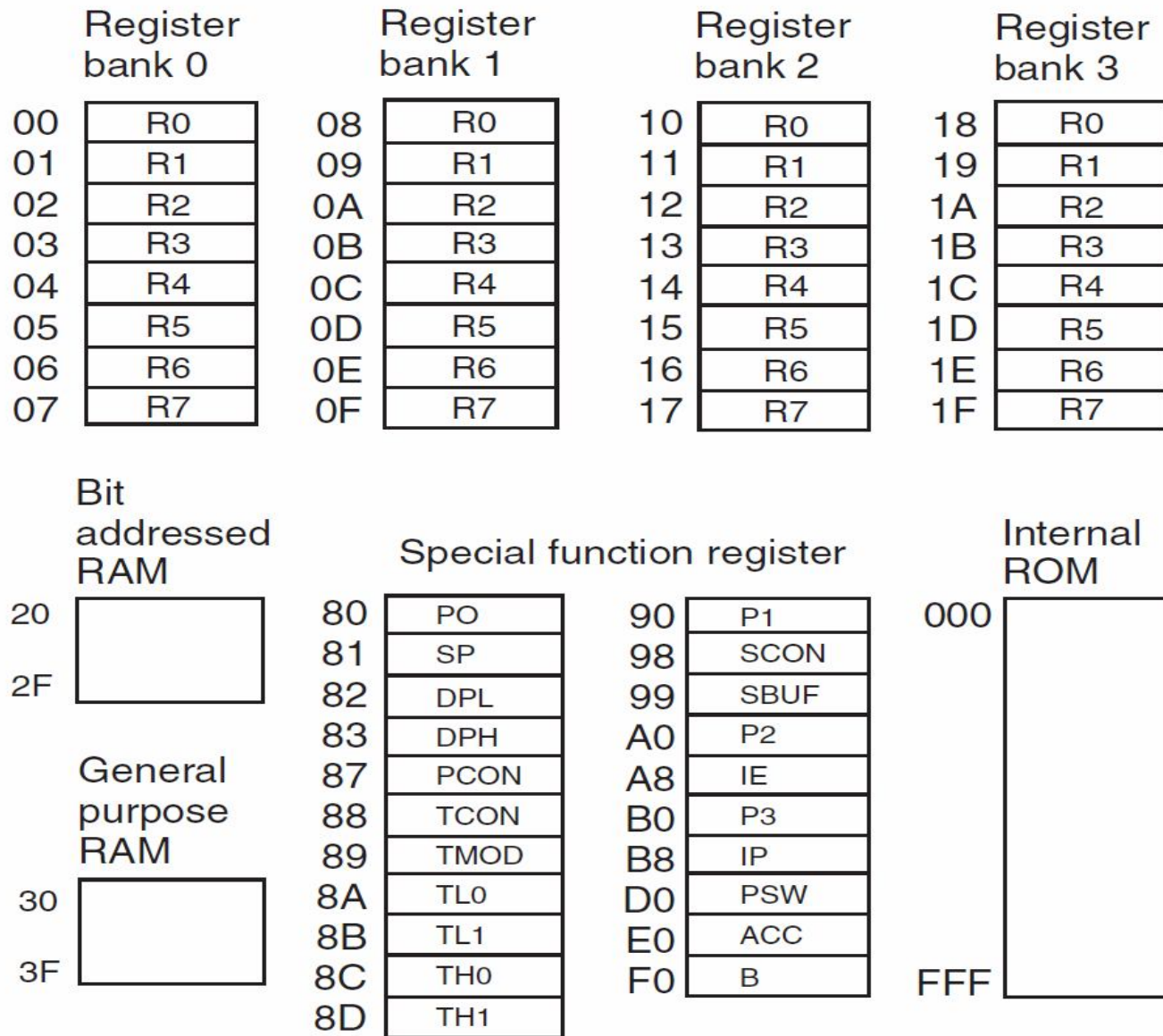


Figure C.3 80C51 programming model

8051 Stack and Stack pointer

- The **stack** is a section of RAM used by the CPU to store information **temporarily**.
 - This information could be data or an address
- The register used to access the stack is called the **SP (stack pointer) register**
 - The stack pointer in the 8051 is **only 8 bit wide**, which means that it can take value of 00 to FFH
 - When the 8051 is powered up (i.e.,) reset, the SP register contains value 07
 - RAM location 08 is the first location begin used for the stack by the 8051

8051 Stack and Stack pointer

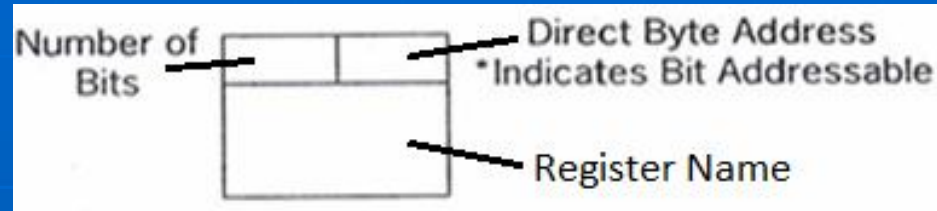
- The storing of a CPU register in the stack is called a **PUSH**
 - SP is pointing to the last used location of the stack
 - As we push data onto the stack, the **SP is incremented** by one
 - This is **different** from many microprocessors
- Loading the contents of the stack back into a CPU register is called a **POP**
 - With every pop, the top byte of the stack is copied to the register specified by the instruction and the stack pointer is **decremented** once

Special Function Registers

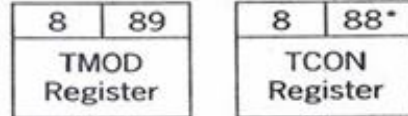
- 80h to FFh are used for SFRs
- PC is not part of SFR.

Name	Function	Name	Function
A	Accumulator	SBUF	Serial Port data buffer
B	Arithmetic	SP	Stack Pointer
DPH	Addressing Ext Memory	TMOD	Timer/Counter mode cntrl
DPL	Addressing Ext Memory	TCON	Timer/Counter cntrl
IE	Interrupt enable	TL0	Timer0 lower byte
IP	Interrupt Priority	TH0	Timer0 higher byte
P0	I/O Port Latch	TL1	Timer1 lower byte
P1	I/O Port Latch	TH1	Timer1 higher byte
P2	I/O Port Latch		
P3	I/O Port Latch		
PCON	Power Control		
PSW	Pgm Status Word		
SCON	Serial PortCntrl		

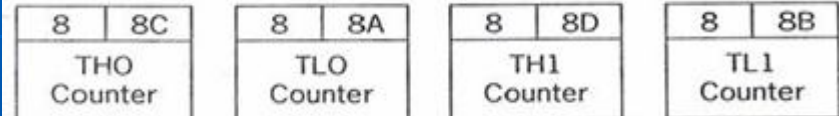
Special Function Registers [SFR]



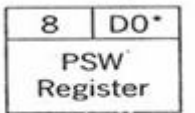
Math Registers



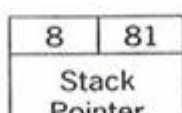
Timer Control Registers



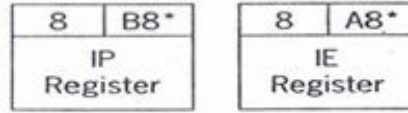
Timer/Counter Registers



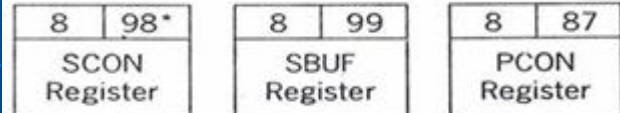
Flags



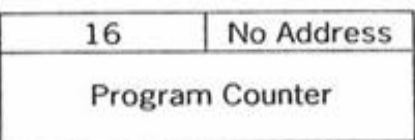
Stack Pointer



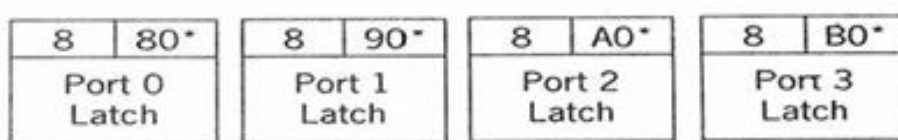
Interrupt Registers



Serial Data Registers



Program Counter

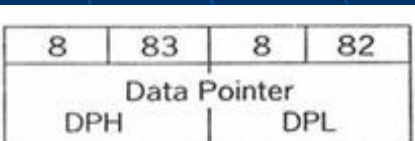


Port 0 Latch

Port 1 Latch

Port 2 Latch

Port 3 Latch



Data Pointer
DPH DPL