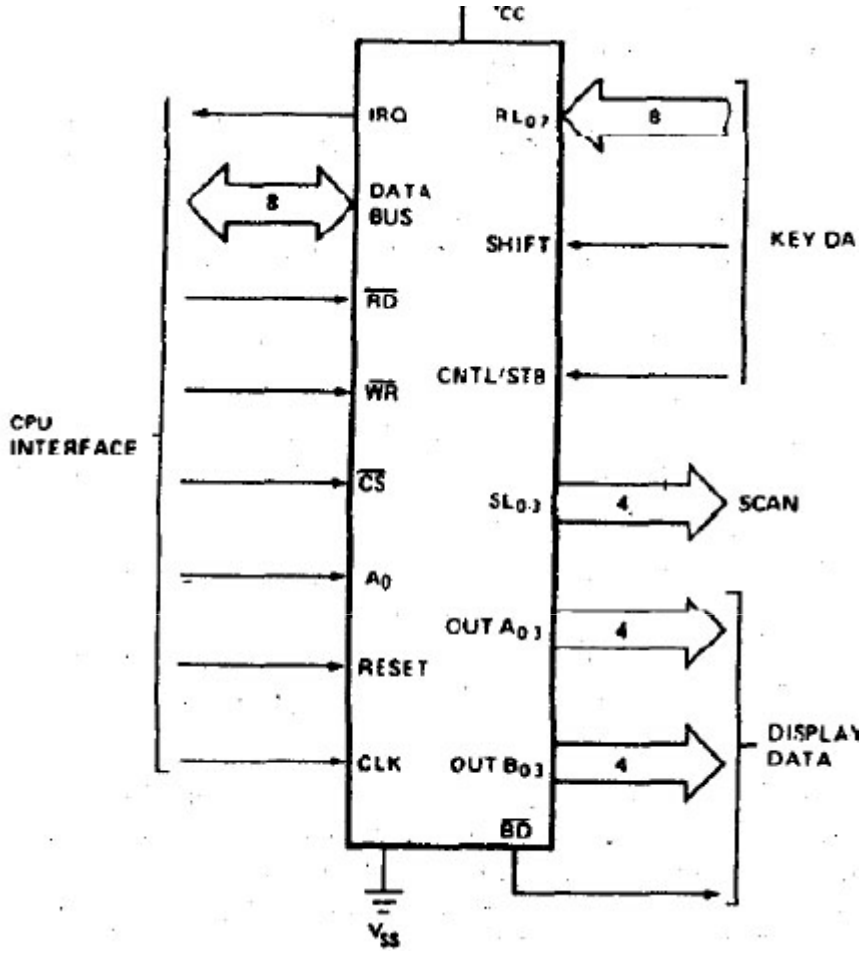
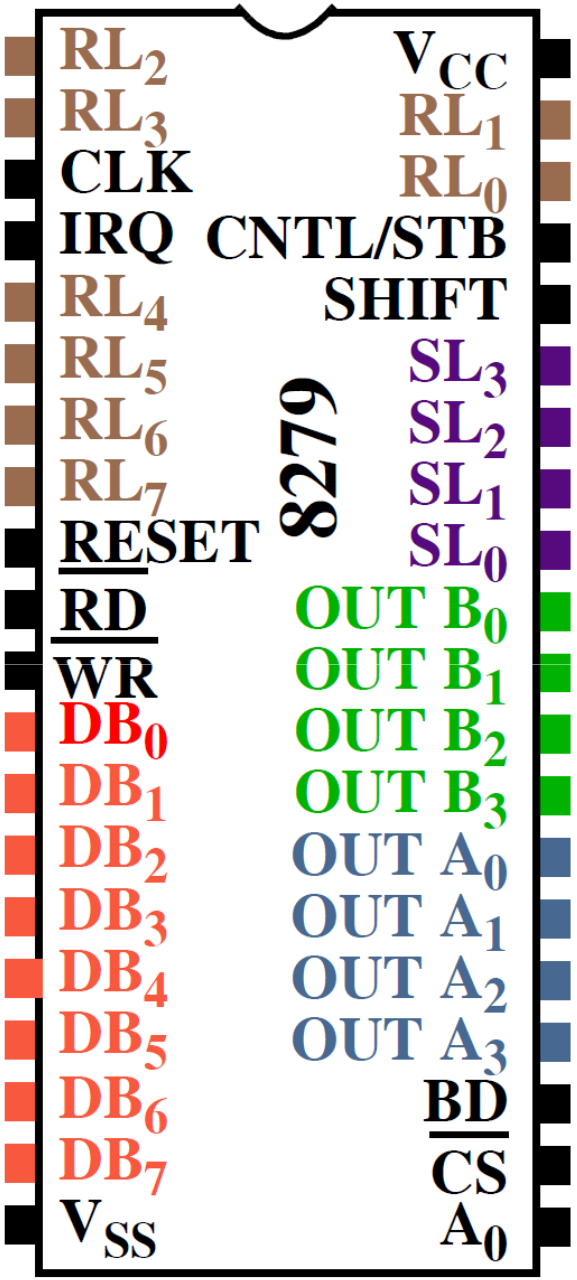
8279- Keyboard Display Controller

Features of 8279

- Scans and encodes up to a 64-key keyboard.
- Controls up to a 16-digit numerical display.
- Keyboard has a built-in FIFO 8 character buffer to store the keyboard Entries and an Interrupt signal with each Entry.
- The display is controlled from an internal 16x8 RAM that stores the coded display information.


CPU INTERFACE
IRQ
DATA BUS
RD
WR
CS
A0
RESET
CLK
VCC
RL0-7
SHIFT
CNTL/STB
SL0-3
OUT A0-3
OUT B0-3
BD
VSS
8
4
KEY DA
SCAN
DISPLAY DATA


RL2
RL3
CLK
IRQ
RL4
RL5
RL6
RL7
RESET
RD
WR
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
VSS
8279
VCC
RL1
RL0
CNTL/STB
SHIFT
SL3
SL2
SL1
SL0
OUT B0
OUT B1
OUT B2
OUT B3
OUT A0
OUT A1
OUT A2
OUT A3
BD
CS
A0

Pin Details

- **A0** : Selects data (0) or control/status (1) for reads and writes between microprocessor and 8279.
- **BD** : Output that blanks the displays.
- **CLK** : Used internally for timing. Maximum is 3 MHz
- **CN/ST** : Control/strobe, connected to the control key on the keyboard.
- **CS** : Chip select that enables programming, reading the keyboard, etc.
- **DB7-DB0** : Consists of bidirectional pins that connect to data bus on micro.

Pin Details

- **IRQ** : Interrupt request, becomes 1 when a key is pressed, data is available.
- **OUT A3-A0/B3-B0** : Outputs that sends data to the most significant/least significant nibble of display.
- **RD(WR)** : Connects to micro's IORC or RD signal, reads data/status registers.
- **RESET** : Connects to system RESET.
- **RL7-RL0** : Return lines are inputs used to sense key depression in the keyboard matrix.
- **Shift** : Shift connects to Shift key on keyboard.
- **SL3-SL0** : Scan line outputs scan both the keyboard and displays.

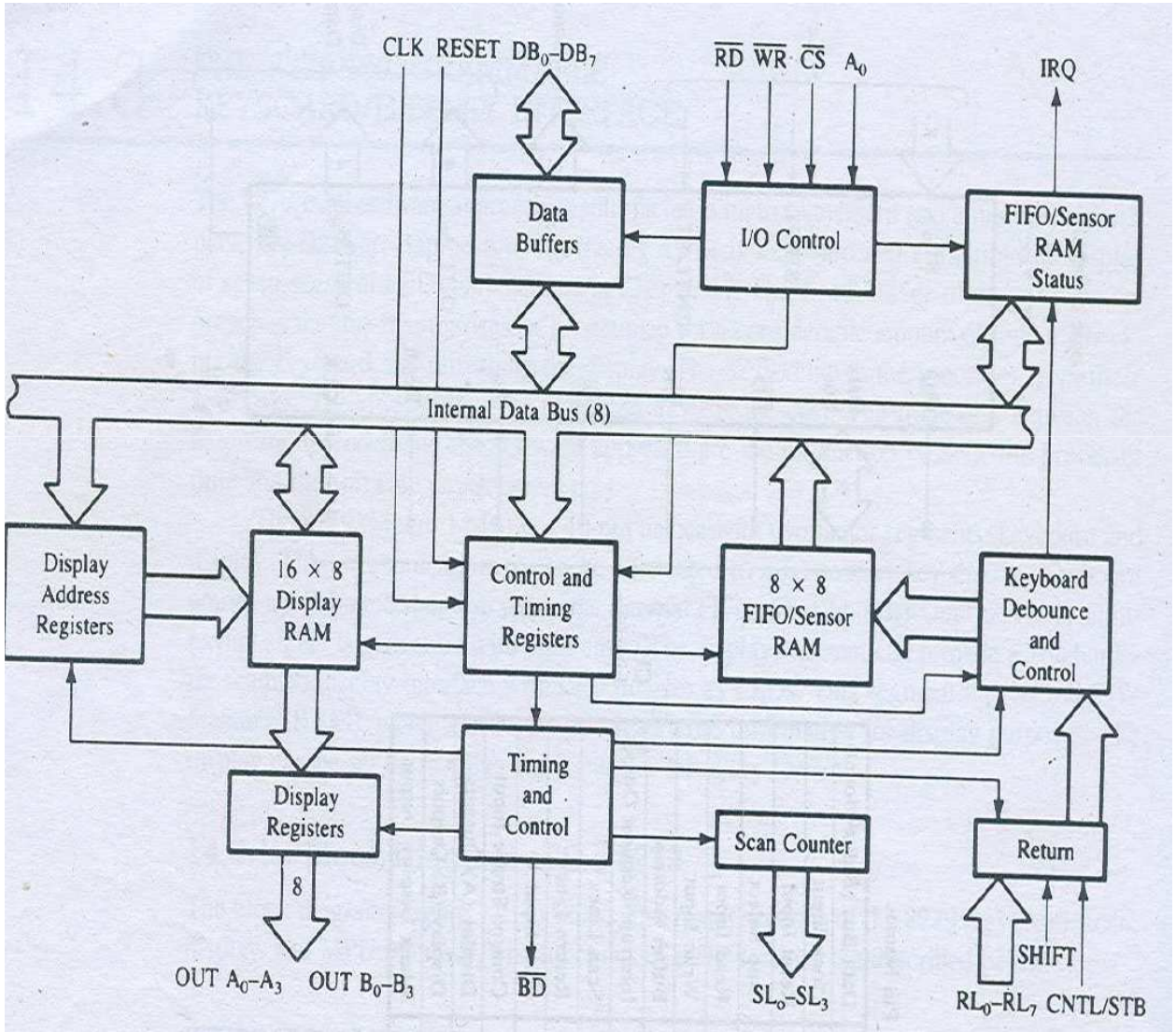
Input Modes

- Scanned Keyboard—with encoded (8 x 8 key keyboard) or decoded (4 x 8 key keyboard) scan lines. A key depression generates a 6-bit encoding of key position. Position and shift and control status are stored in the FIFO. Keys are automatically debounced with 2-key lockout or N-key rollover.
- Scanned Sensor Matrix—with encoded (8 x 8 matrix switches) or decoded (4 x 8 matrix switches) scan lines. Key status (open or closed) stored in RAM addressable by CPU.
- Strobed Input—Data on return lines during control line strobe is transferred to FIFO.

Output Modes

- 8 or 16 character multiplexed displays that can be organized as dual 4-bit or single 8-bit (B_0 = D_0, A_3 = D_7).
- Right entry or left entry display formats.

8279 Block Diagram



Block Diagram

Mainly 4 Sections:

1.KeyBoard Section

2.Scan Section

3.Display Section

4. µp Interface Section

Keyboard Section

- RL0 – RL7 connected to 8 columns of keyboard
- 2 modes: 2-key lockout

  N key Rollover
- FIFO RAM with 8 registers to store 8 keyboard entries and each read in the order of their entries.
- Sent IRQ signal when FIFO is not empty

Scan Section

- It has a Scan Counter and 4 Scan Lines
- Connected to 4 – to – 16 Decoder to generate 16 scan lines
- Scan lines can be connected to rows of Matrix Keyboard and Digit drivers of Display

Display Section

- 8 Output lines divided into 2 groups:

  A0 – A3 and B0 – B3

- Can be used as 8 or 4/4
- $\overline{BD}$ line for display Blanking
- 16 X 8 Display RAM

µp Interface Section

- Data bus : DB0 – DB7
- One IRQ Line
- Six interface lines and A0
- A0 = 1 ; signals are control/status word

8279 COMMAND WORDS (A0 = 1)

1. Keyboard/Display Mode
2. Program Clock
3. Read FIFO/Sensor RAM
4. Read Display RAM
5. Write Display RAM
6. Display write inhibit /Blanking
7. Clear
8. End Interrupt/Error mode set

D7,D6,D5 Configurations

D7	D6	D5	Function	Purpose
0	0	0	Mode set	Selects the number of display positions, type of key scan...
0	0	1	Clock	Programs internal clk, sets scan and debounce times.
0	1	0	Read FIFO	Selects type of FIFO read and address of the read.
0	1	1	Read Display	Selects type of display read and address of the read.
1	0	0	Write Display	Selects type of write and the address of the write.
1	0	1	Display write inhibit	Allows half-bytes to be blanked.
1	1	0	Clear	Clears the display or FIFO
1	1	1	End interrupt	Clears the IRQ signal to the microprocessor.

Keyboard/Display Mode Set

	MSB							LSB
Code:	0	0	0	D	D	K	K	K

Where DD is the Display Mode and KKK is the Keyboard Mode.

DD

0	0	8 8-bit character display—Left entry
0	1	16 8-bit character display—Left entry*
1	0	8 8-bit character display—Right entry
1	1	16 8-bit character display—Right entry

KKK			
0	0	0	Encoded Scan Keyboard—2 Key Lock-out*
0	0	1	Decoded Scan Keyboard—2-Key Lock-out
0	1	0	Encoded Scan Keyboard—N-Key Roll-over
0	1	1	Decoded Scan Keyboard—N-Key Roll-over
1	0	0	Encoded Scan Sensor Matrix
1	0	1	Decoded Scan Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

Program Clock

Code:

0	0	1	P	P	P	P	P

All timing and multiplexing signals for the 8279 are generated by an internal prescaler. This prescaler divides the external clock (pin 3) by a programmable integer. Bits PPPPP determine the value of this integer which ranges from 2 to 31.

Read FIFO/Sensor RAM

Code:

0	1	0	AI	X	A	A	A

X = Don't Care

The CPU sets the 8279 for a read of the FIFO/Sensor RAM by first writing this command. In the Scan Keyboard Mode, the Auto-Increment flag (AI) and the RAM address bits (AAA) are irrelevant. The 8279 will automatically drive the data bus for each subsequent read ($A_0 = 0$) in the same sequence in which the data first entered the FIFO. All subsequent reads will be from the FIFO until another command is issued.

In the Sensor Matrix Mode, the RAM address bits AAA select one of the 8 rows of the Sensor RAM. If the AI flag is set (AI = 1), each successive read will be from the subsequent row of the sensor RAM.

Read Display RAM

Code:	0	1	1	AI	A	A	A	A

The CPU sets up the 8279 for a read of the Display RAM by first writing this command. The address bits AAAA select one of the 16 rows of the Display RAM. If the AI flag is set (A1 = 1), this row address will be incremented after each following read *or write* to the Display RAM. Since the same counter is used for both reading and writing, this command sets the next read or *write* address and the sense of the Auto-Increment mode for both operations.

Write Display RAM

Code:	1	0	0	AI	A	A	A	A

The CPU sets up the 8279 for a write to the Display RAM by first writing this command. After writing the command with $A_0 = 1$, all subsequent writes with $A_0 = 0$ will be to the Display RAM. The addressing and Auto-Increment functions are identical to those for the Read Display RAM. However, this command does not affect the source of subsequent Data Reads; the CPU will read from whichever RAM (Display of FIFO/Sensor) which was last specified. If, indeed, the Display RAM was last specified, the Write Display RAM will, nevertheless, change the next Read location.

Display Write Inhibit/Blanking

					A	B	A	B
Code:	1	0	1	X	IW	IW	BL	BL

The IW Bits can be used to mask nibble A and nibble B in applications requiring separate 4-bit display ports. By setting the IW flag (IW = 1) for one of the ports, the port becomes marked so that entries to the Display RAM from the CPU do not affect that port.

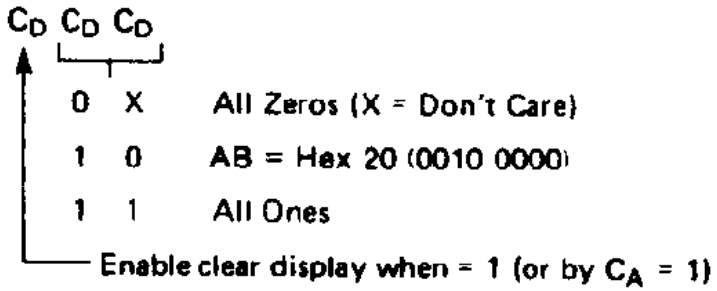
If the user wishes to blank the display, the BL flags are available for each nibble. The last Clear command issued determines the code to be used as a "blank." This code defaults to all zeros after a reset. Note that both BL flags must be set to blank a display formatted with a single 8-bit port.

Clear

Code:

1	1	0	C_D	C_D	C_D	C_F	C_A

The C_D bits are available in this command to clear all rows of the Display RAM to a selectable blanking code as follows:



If the C_F bit is asserted ($C_F = 1$), the FIFO status is cleared and the interrupt output line is reset. Also, the Sensor RAM pointer is set to row 0.

C_A, the Clear All bit, has the combined effect of C_D and C_F; it uses the C_D clearing code on the Display RAM and also clears FIFO status. Furthermore, it resynchronizes the internal timing chain.

End Interrupt/Error Mode Set

Code:

1	1	1	E	X	X	X	X

X = Don't care

For the sensor matrix modes this command lowers the IRQ line and enables further writing into RAM.

For the N-key rollover mode—if the E bit is programmed to "1" the chip will operate in the special Error mode.

Interfacing with 8086