DMA Controlller – 8257/8237

Direct memory access

- Direct memory access (DMA) is a process in which an external device takes over the control of system bus from the CPU.

- DMA is for high-speed data transfer from/to mass storage peripherals, e.g. harddisk drive, magnetic tape, CD-ROM, and sometimes video controllers.

- The basic idea of DMA is to transfer blocks of data directly between memory and peripherals.

- The data don’t go through the microprocessor but the data bus is occupied.

Basic process of DMA – Minimum Mode

- The **HOLD** and **HLDA** pins are used to receive and acknowledge the hold request respectively.
- Normally the CPU has full control of the system bus.
- In a DMA operation, the peripheral takes over bus control temporarily.

Basic process of DMA – Maximum Mode

- The **RQ/GT1** and **RQ/GT0** pins are used to issue DMA request and receive acknowledge signals.

- Sequence of events of a typical DMA process:

  1. *Peripheral asserts one of the request pins, e.g. RQ/GT1 or RQ/GT0 (RQ/GT0 has higher priority)*

  2. *8086 completes its current bus cycle and enters into a HOLD state.*

  3. *8086 grants the right of bus control by asserting a grant signal via the same pin as the request signal.*

  4. *DMA operation starts.*

  5. *Upon completion of the DMA operation, the peripheral asserts the request/grant pin again to relinquish bus control.*

DMA controller

- A DMA controller interfaces with several peripherals that may request DMA.

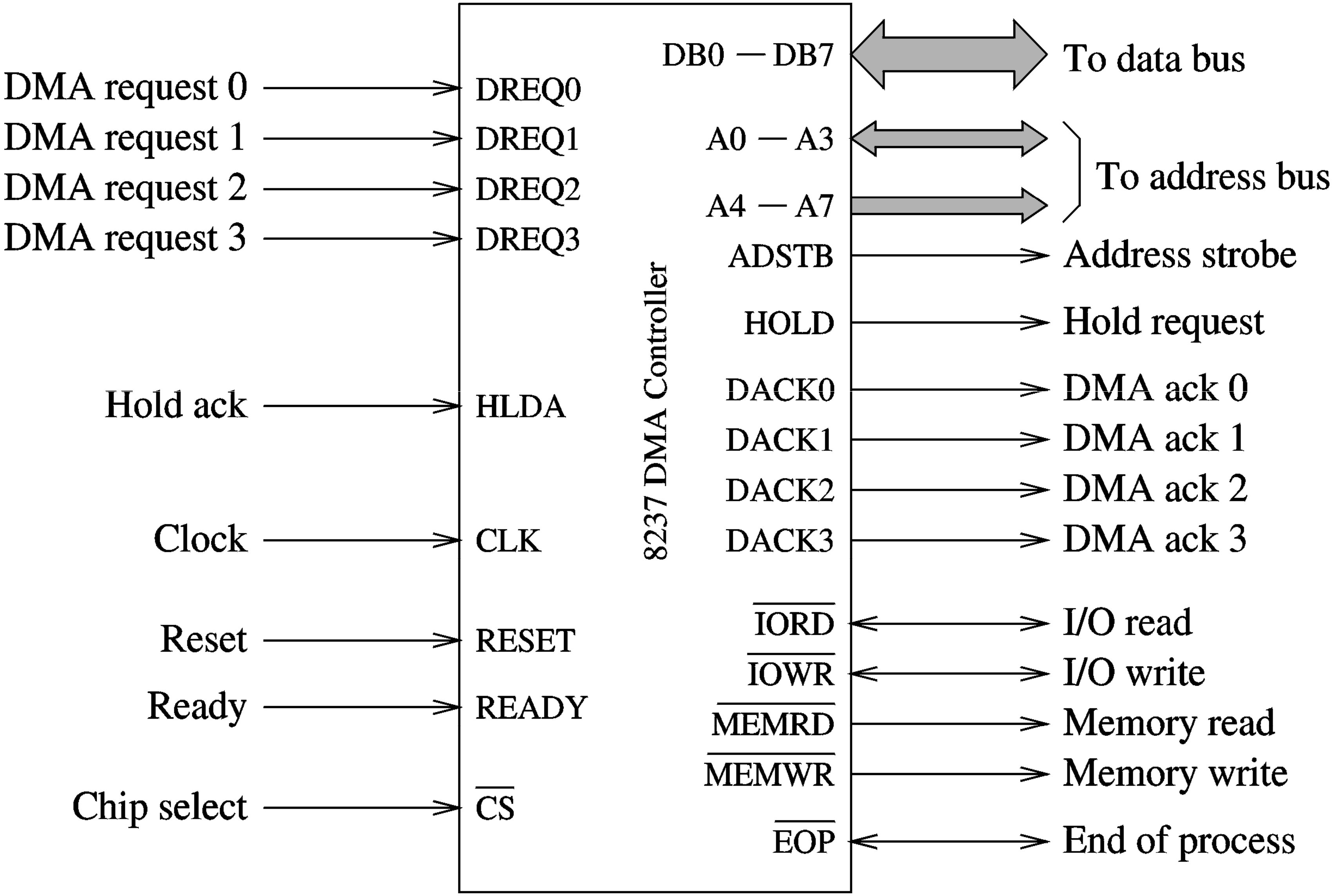
- The controller decides the priority of simultaneous DMA requests communicates with the peripheral and the CPU, and provides memory addresses for data transfer.

- DMA controller commonly used with 8086 is the 8257/8237 programmable device.

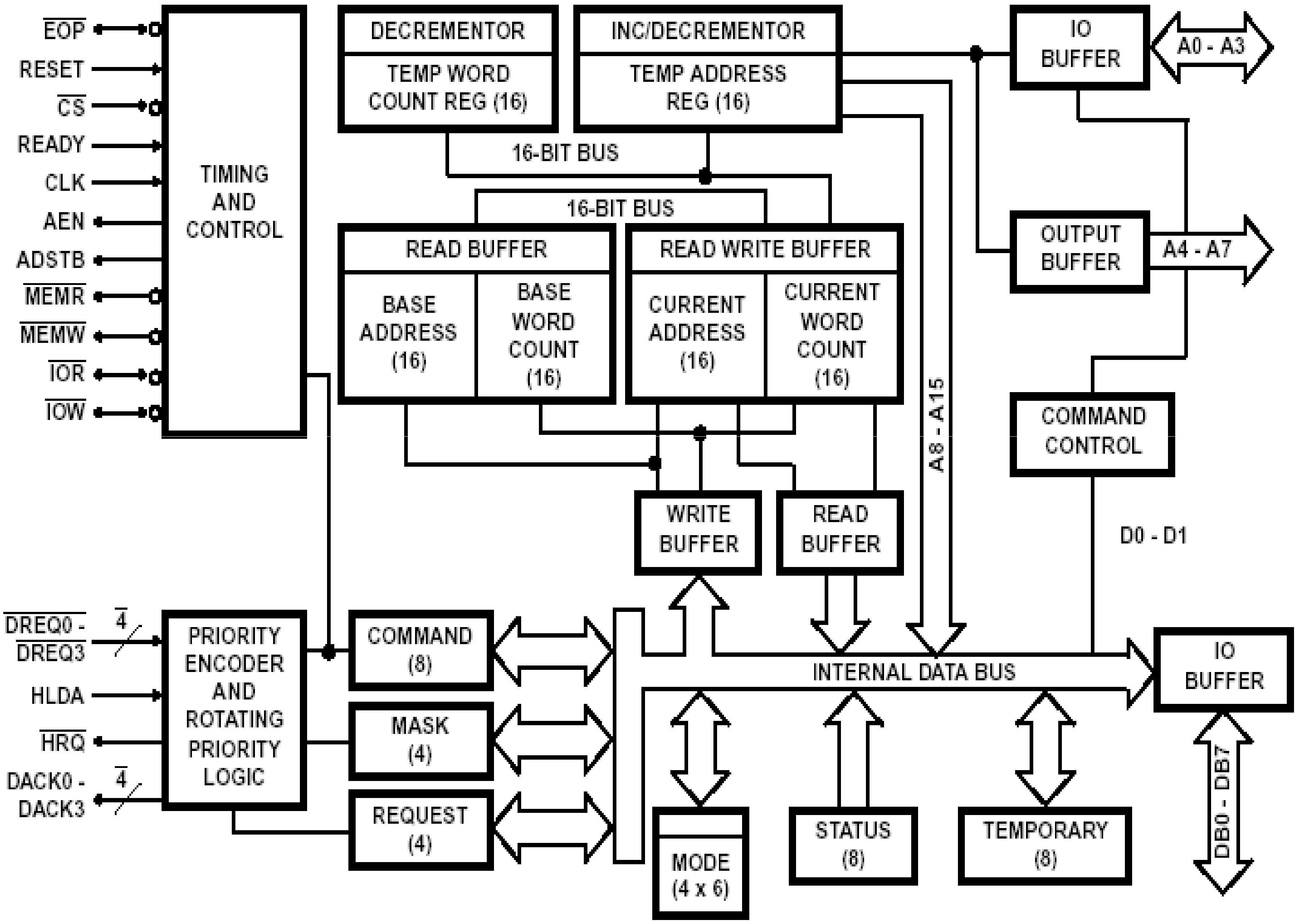
- The 8257/8237 is a 4-channel device.

- Each channel is dedicated to a specific peripheral device and capable of addressing 64 K bytes section of memory.

8237 - DMA Controller



Block Diagram



8237 Registers

1. **Current word register**
2. **Command register**
3. **Mode register**
4. **Request register**
5. **Mask register**
6. **Status register**
7. **Temporary register**
8. **Current address register**

8237 Registers

1.Current address register

- One 16-bit register for each channel
- Holds address for the current DMA transfer

2.Current word register

- Keeps the byte count
- Generates terminal count (TC) signal when the count goes from zero to FFFFH

3.Command register

- Used to program 8257

8237 Registers

4.Mode register

- Each channel can be programmed to
  - Read or write
  - Autoincrement or autodecrement the address
  - Autoinitialize the channel

5.Request register

- For software-initiated DMA

6.Mask register

- Used to disable a specific channel

7.Status register

8.Temporary register

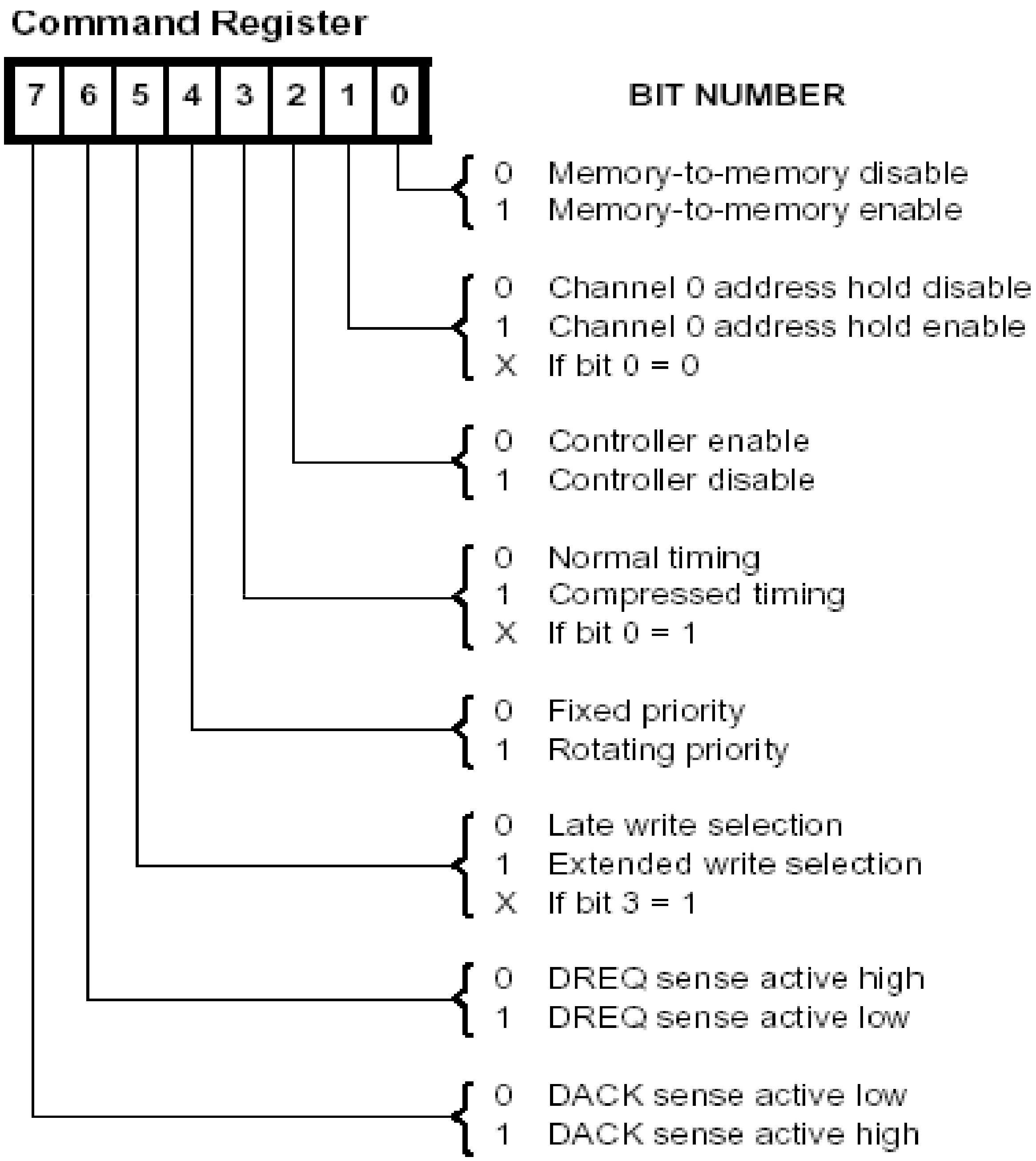
- Used for memory-to-memory transfers

Types of data transfer

- 8237 supports **four** types of data transfer

1. **Single cycle transfer**
   - Only single transfer takes place
   - Useful for slow devices
2. **Block transfer mode**
   - Transfers data until TC is generated or external EOP signal is received
3. **Demand transfer mode**
   - Similar to the block transfer mode
   - In addition to TC and EOP, transfer can be terminated by deactivating DREQ signal
4. **Cascade mode**
   - Useful to expand the number channels beyond four

Command Register



Command Register

7 6 5 4 3 2 1 0

BIT NUMBER

0 Memory-to-memory disable
1 Memory-to-memory enable

0 Channel 0 address hold disable
1 Channel 0 address hold enable
X If bit 0 = 0

0 Controller enable
1 Controller disable

0 Normal timing
1 Compressed timing
X If bit 0 = 1

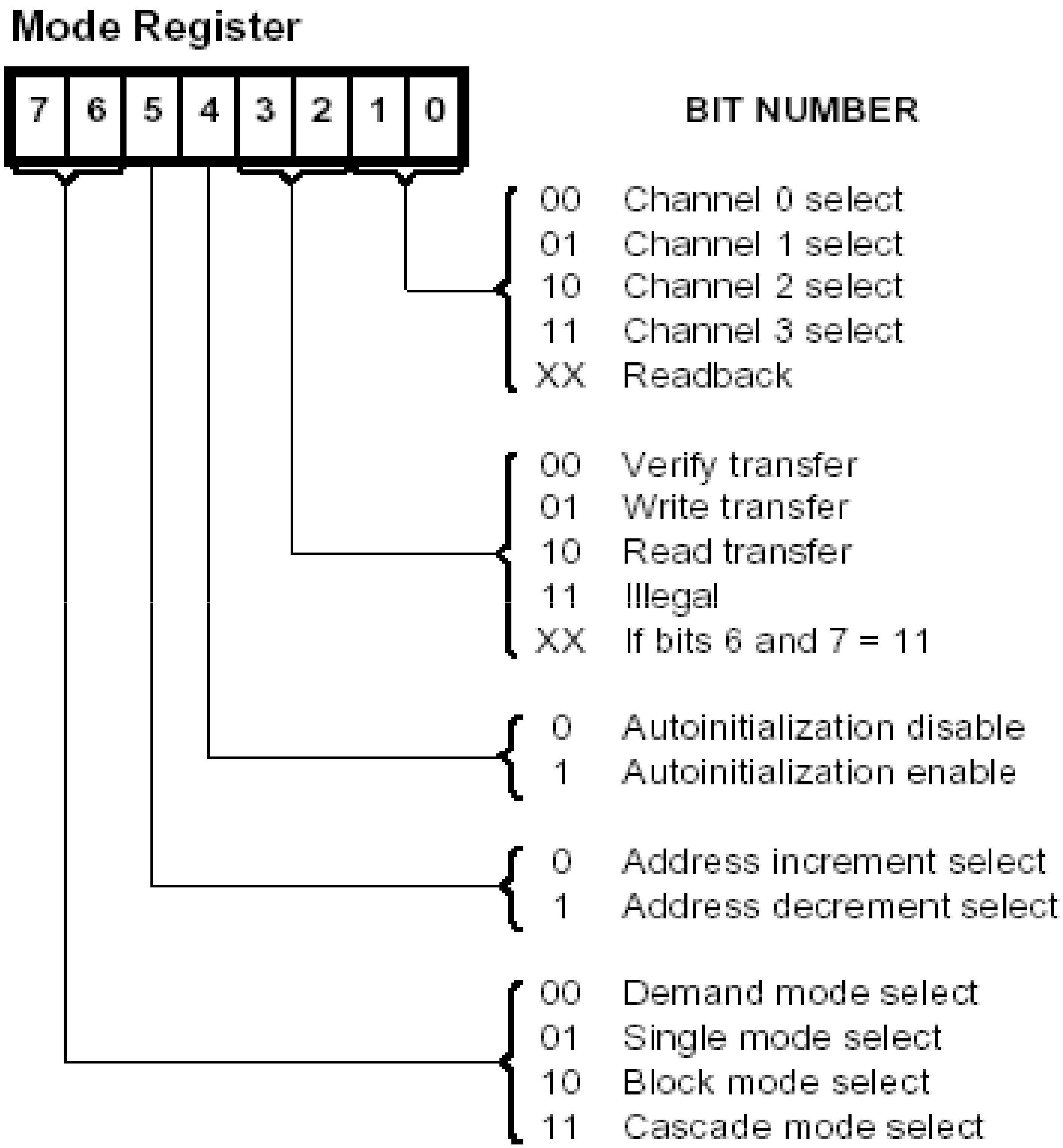
0 Fixed priority
1 Rotating priority

0 Late write selection
1 Extended write selection
X If bit 3 = 1

0 DREQ sense active high
1 DREQ sense active low

0 DACK sense active low
1 DACK sense active high

Mode Register



Mode Register

7	6	5	4	3	2	1	0

BIT NUMBER

00 Channel 0 select
01 Channel 1 select
10 Channel 2 select
11 Channel 3 select
XX Readback

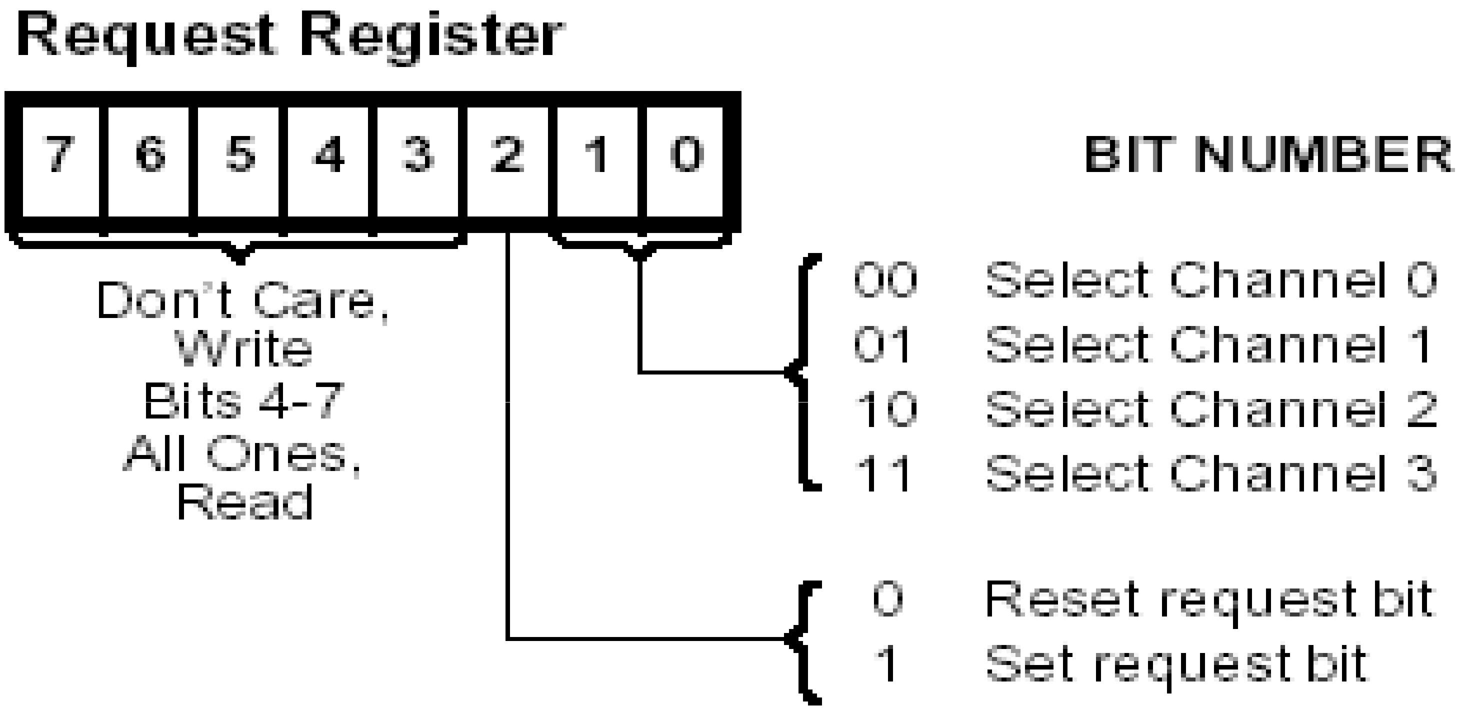
00 Verify transfer
01 Write transfer
10 Read transfer
11 Illegal
XX If bits 6 and 7 = 11

0 Autoinitialization disable
1 Autoinitialization enable

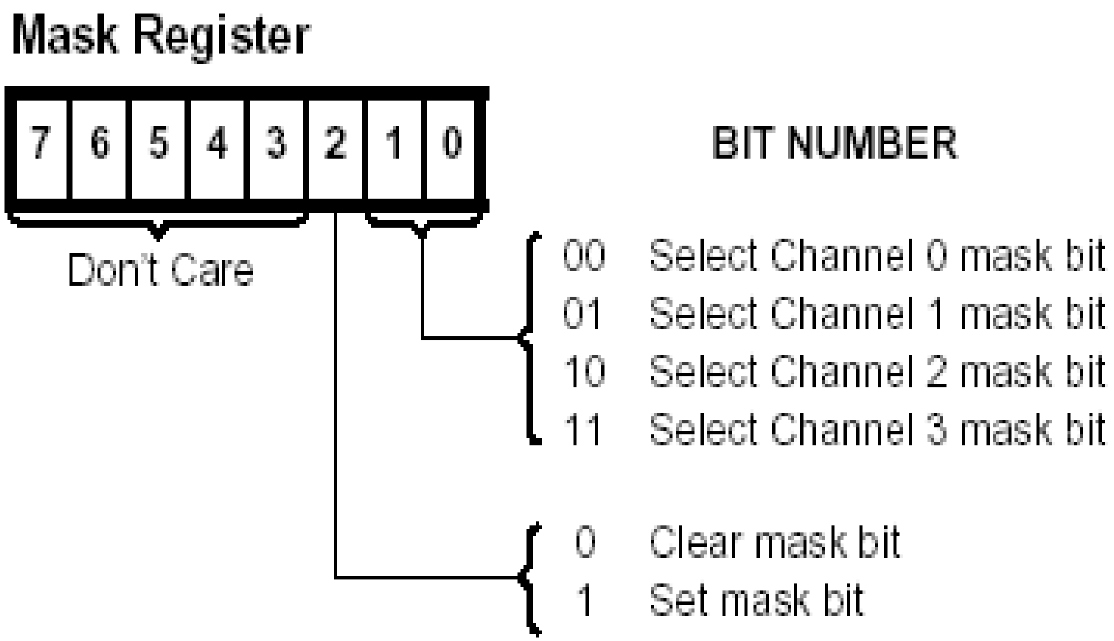
0 Address increment select
1 Address decrement select

00 Demand mode select
01 Single mode select
10 Block mode select
11 Cascade mode select

Request Register



Mask Register



Mask Register

7 6 5 4 3 2 1 0

BIT NUMBER

Don't Care

00 Select Channel 0 mask bit

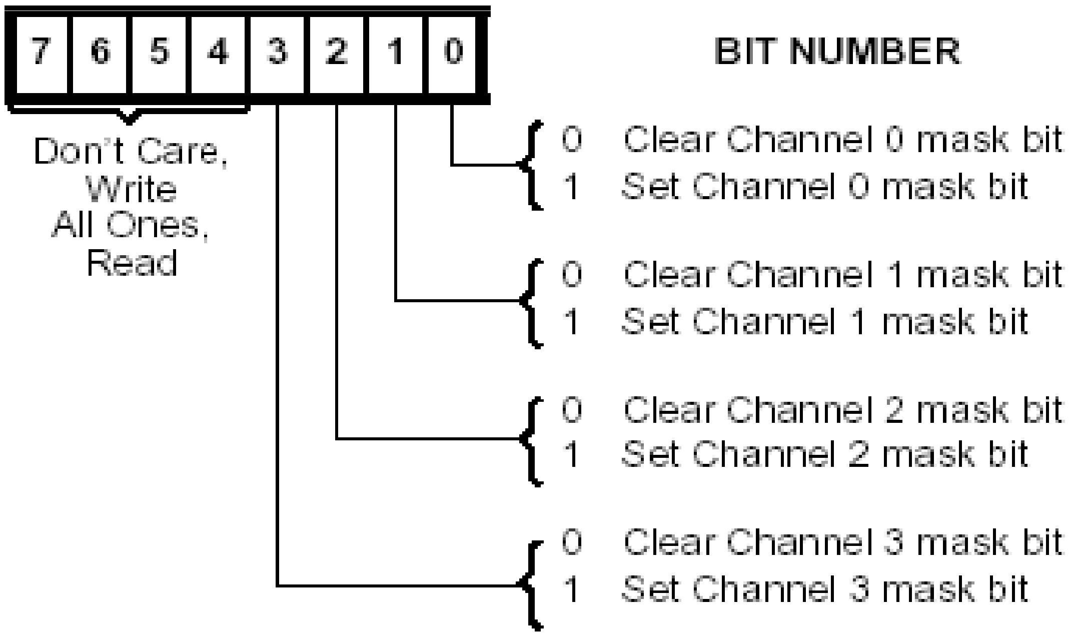
01 Select Channel 1 mask bit

10 Select Channel 2 mask bit

11 Select Channel 3 mask bit

0 Clear mask bit

1 Set mask bit



7 6 5 4 3 2 1 0

BIT NUMBER

Don't Care,
Write
All Ones,
Read

0 Clear Channel 0 mask bit

1 Set Channel 0 mask bit

0 Clear Channel 1 mask bit

1 Set Channel 1 mask bit

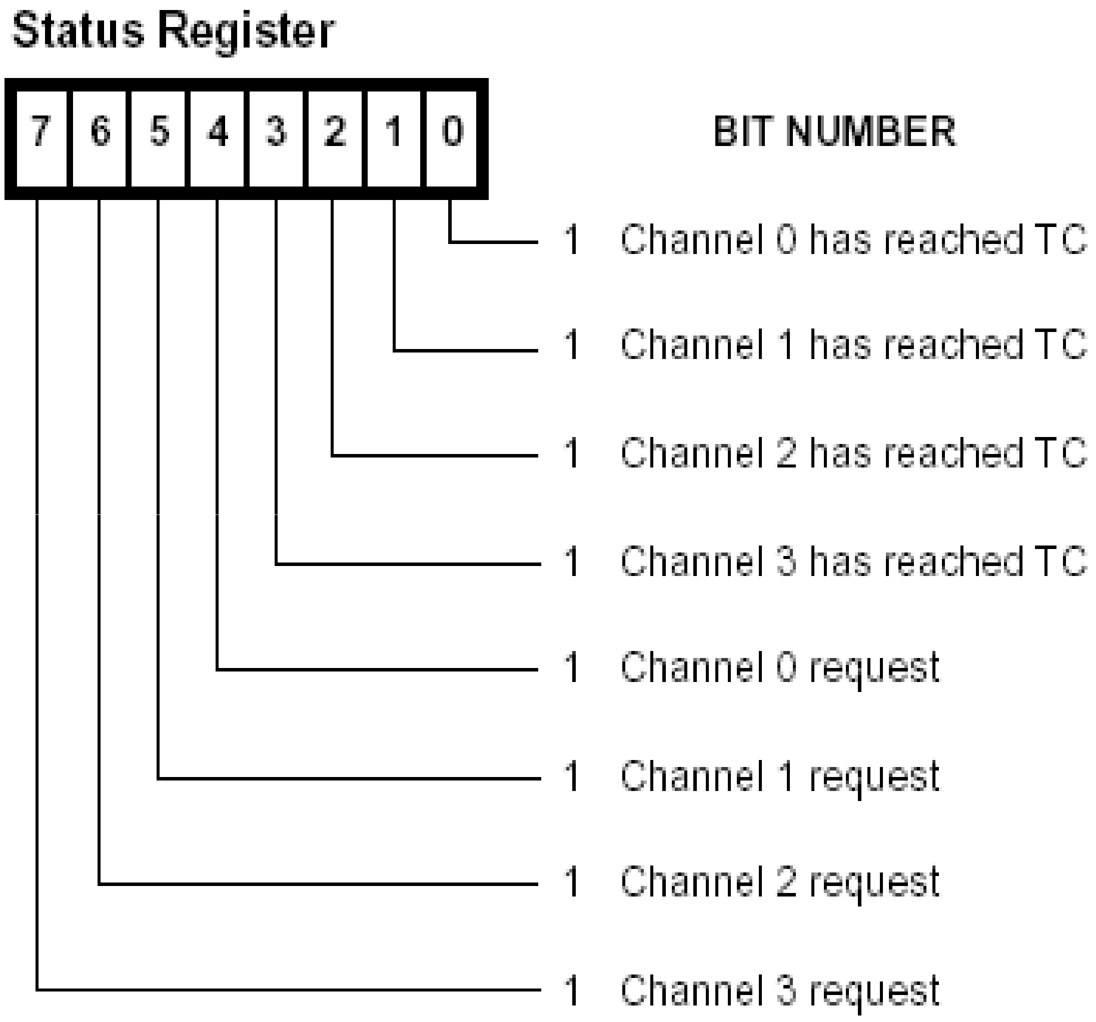
0 Clear Channel 2 mask bit

1 Set Channel 2 mask bit

0 Clear Channel 3 mask bit

1 Set Channel 3 mask bit

Status Register



Status Register

7 6 5 4 3 2 1 0

BIT NUMBER

1 Channel 0 has reached TC

1 Channel 1 has reached TC

1 Channel 2 has reached TC

1 Channel 3 has reached TC

1 Channel 0 request

1 Channel 1 request

1 Channel 2 request

1 Channel 3 request