I/O Processor-8089

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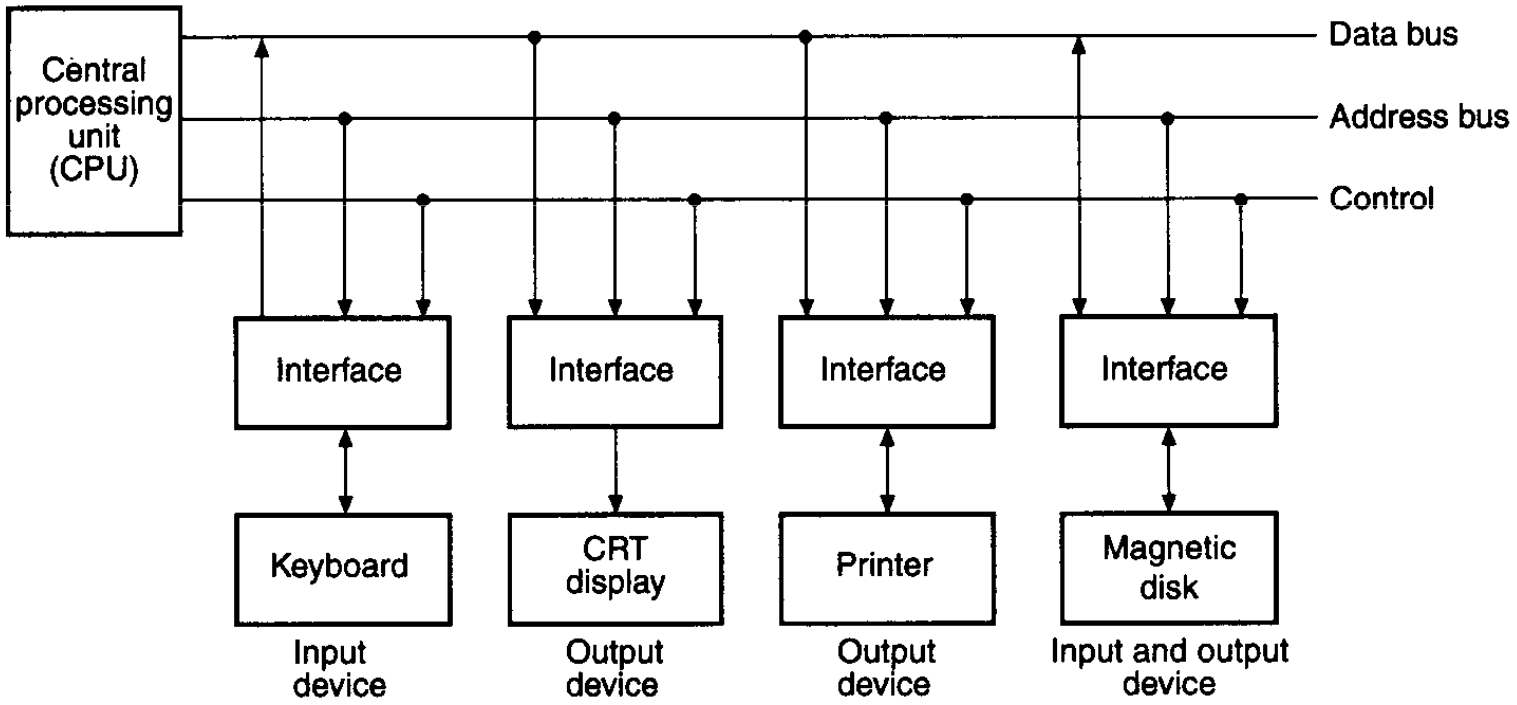
I/O Processors

- I/O Processors handles all of the interactions between the I/O devices and the CPU.
- I/O Processors communicates with input and output devices through separate address, data, and control lines.
- This provides an independent pathway for the transfer of information between external devices and internal memory.
- Relieves the CPU of ‘I/O device chores’

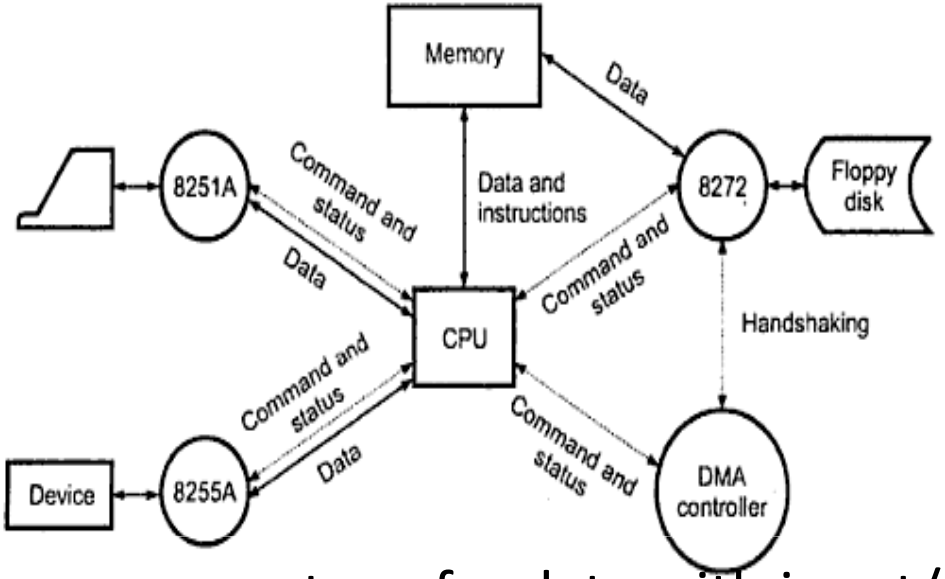
CPU Connection to I/O Devices



I/O Processors

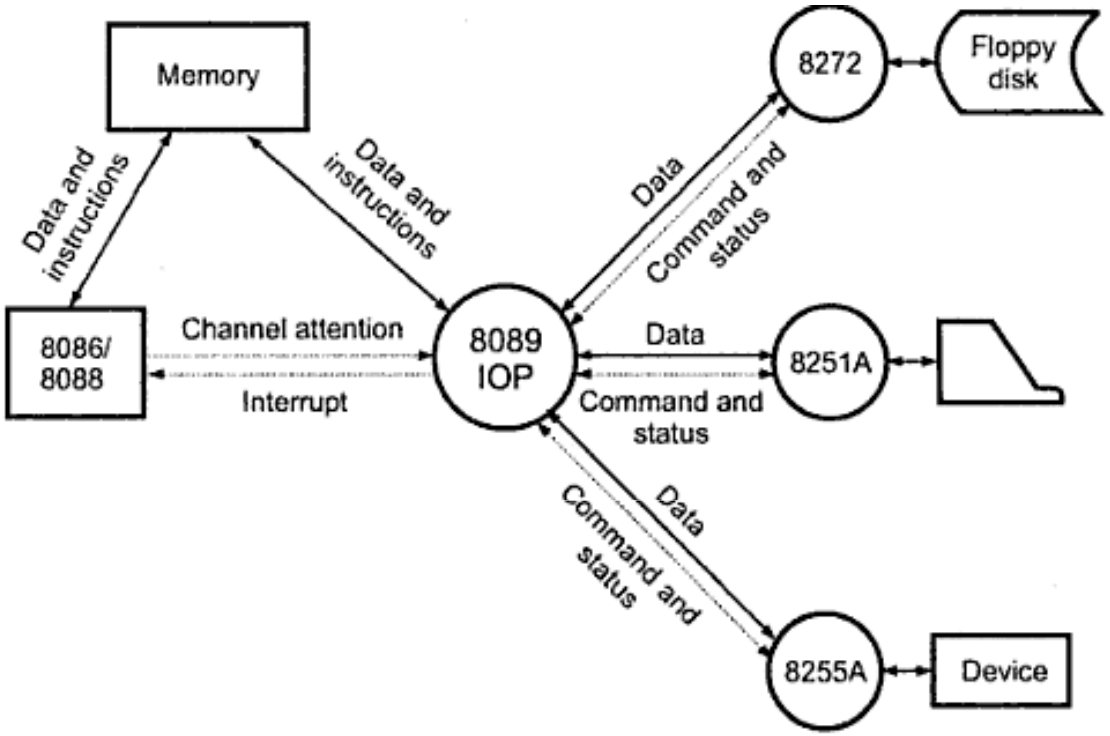
- Communicate directly with all I/O devices
  - Fetch and execute its own instruction
    - IOP instructions are specifically designed to facilitate I/O transfer
    - DMAC must be set up entirely by the CPU
  - Designed to handle the details of I/O processing
- Used to address the problem of direct transfer after executing the necessary format conversion or other instructions
- In an IOP-based system, I/O devices can directly access the memory without intervention by the processor

I/O handled by microprocessor



- Microprocessors can transfer data with input/output port. Here microprocessor is required to set up and perform the actual transfer.
- For high speed data transfer CPU uses the DMA controller to transfer data.
- But microprocessor still needs to set up the device controller, initiate the DMA operation, and examine the post transfer status after the completion of each DMA operation.

I/O handled by IOP

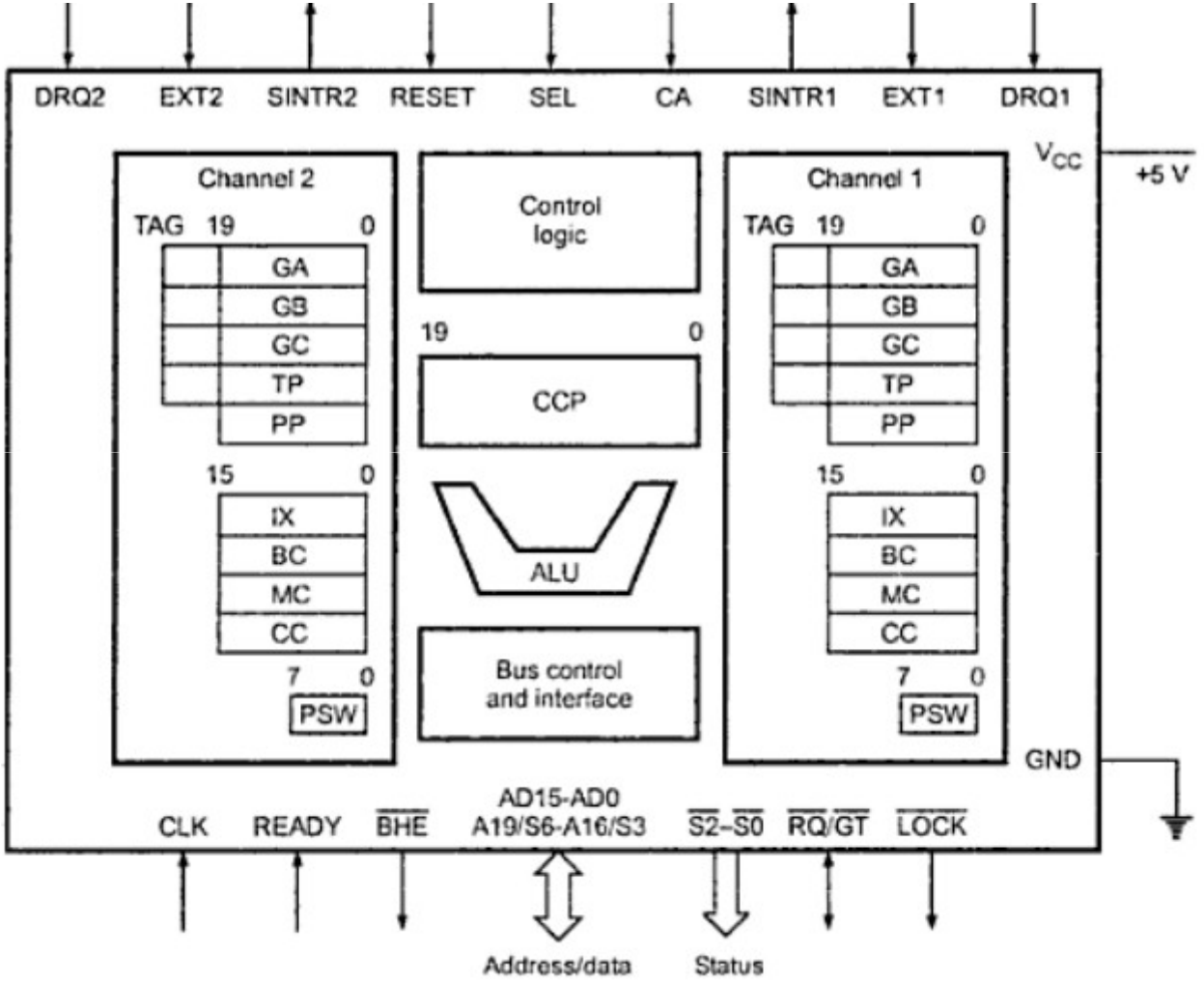


- When I/O is handled by IOP, microprocessor can perform some other function at the time of I/O transfer. This increases the system speed.
- Example: 8089

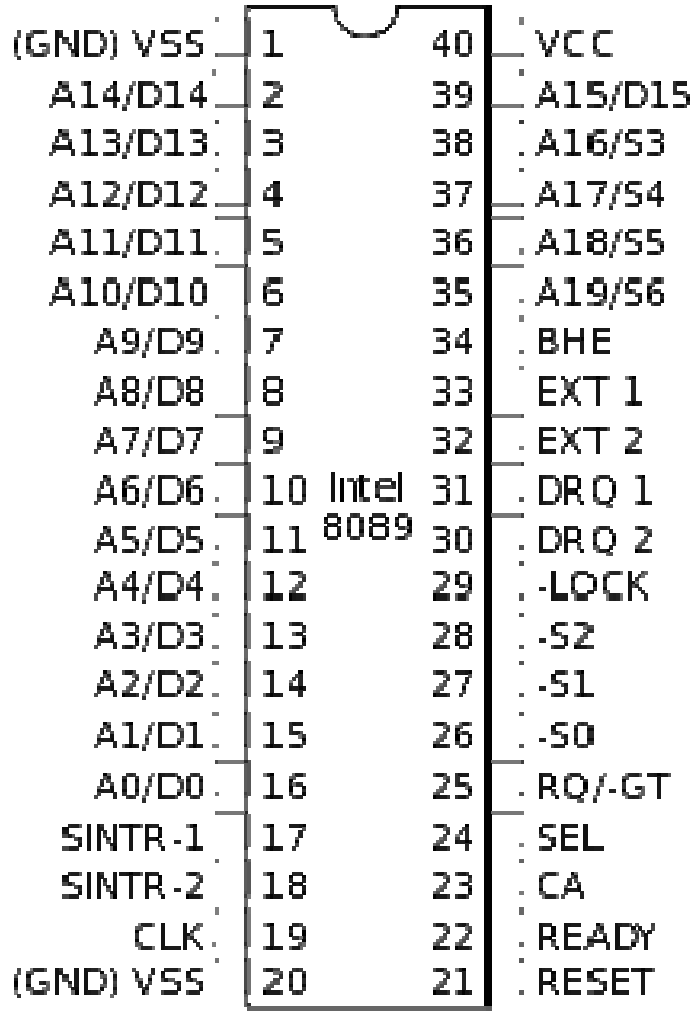
Features of 8089

- An IOP can fetch and execute its own instructions.
- Instructions are specially designed for I/O processing.
- In addition to data transfer, 8089 can perform arithmetic and logic operations, branches, searching and translation.
- IOP does all work involved in I/O transfer including device setup, programmed I/O and DMA operation.
- IOP can transfer data from an 8-bit source to 16-bit destination and vice-versa.
- Communication between IOP and CPU is through memory based control blocks. CPU defines tasks in the control blocks to locate a program sequence, called a channel program.

Internal Block Diagram of 8089



Pin Diagram


(GND) VSS 1
A14/D14 2
A13/D13 3
A12/D12 4
A11/D11 5
A10/D10 6
A9/D9 7
A8/D8 8
A7/D7 9
A6/D6 10
A5/D5 11
A4/D4 12
A3/D3 13
A2/D2 14
A1/D1 15
A0/D0 16
SINTR-1 17
SINTR-2 18
CLK 19
(GND) VSS 20
Intel
8089
40 VCC
39 A15/D15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE
33 EXT 1
32 EXT 2
31 DRQ 1
30 DRQ 2
29 -LOCK
28 -S2
27 -S1
26 -S0
25 RQ/-GT
24 SEL
23 CA
22 READY
21 RESET

Registers of 8089

- GA- Points to source
- GB- Points to destination
- GC-Used as base address of a 256 byte translation table.
- TP-Task pointer
- PP-Parameter pointer
- IX –Index register
- BC
- MC- contains the it pattern to be compared and a mask in bits 15 through 8
- CC-channel control
- PSW-Program status register

Channel control register

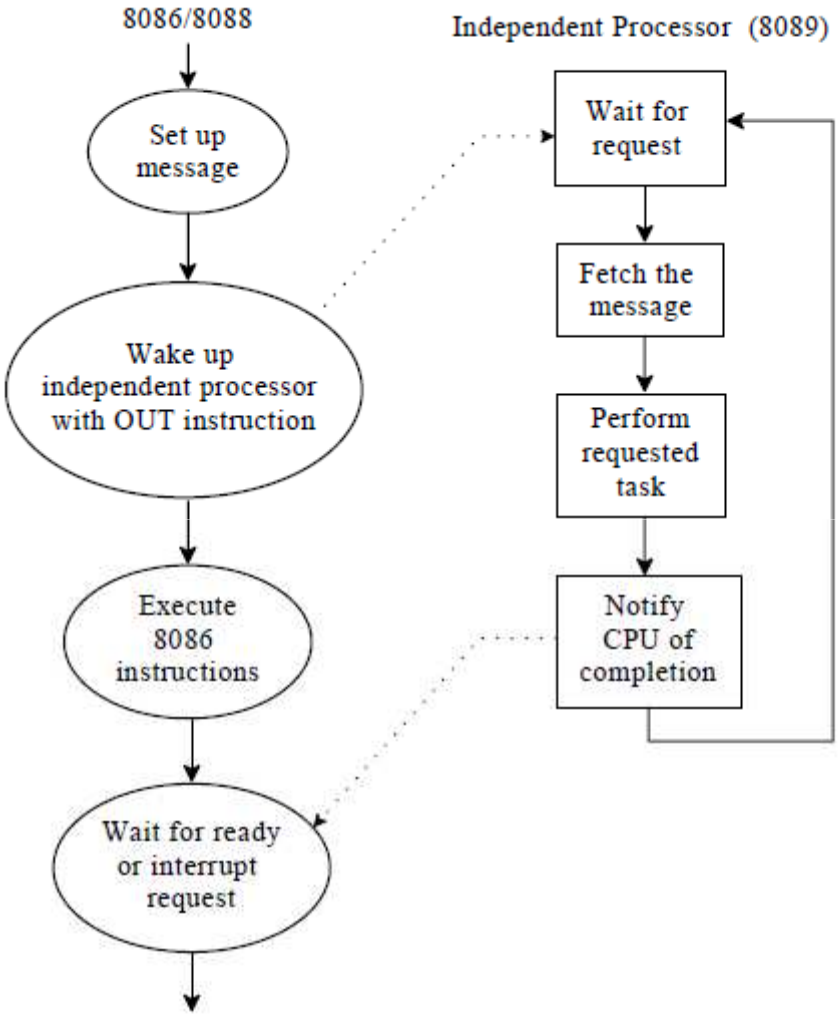
- Function control- b15 & b14
- Translation mode- b13
- Synchronization control-b12 & b11
- Source/ Destination indicator – b10
- Lock control- b9
- Chaining control- b8
- Single transfer mode – b7
- Termination control – b0-b6

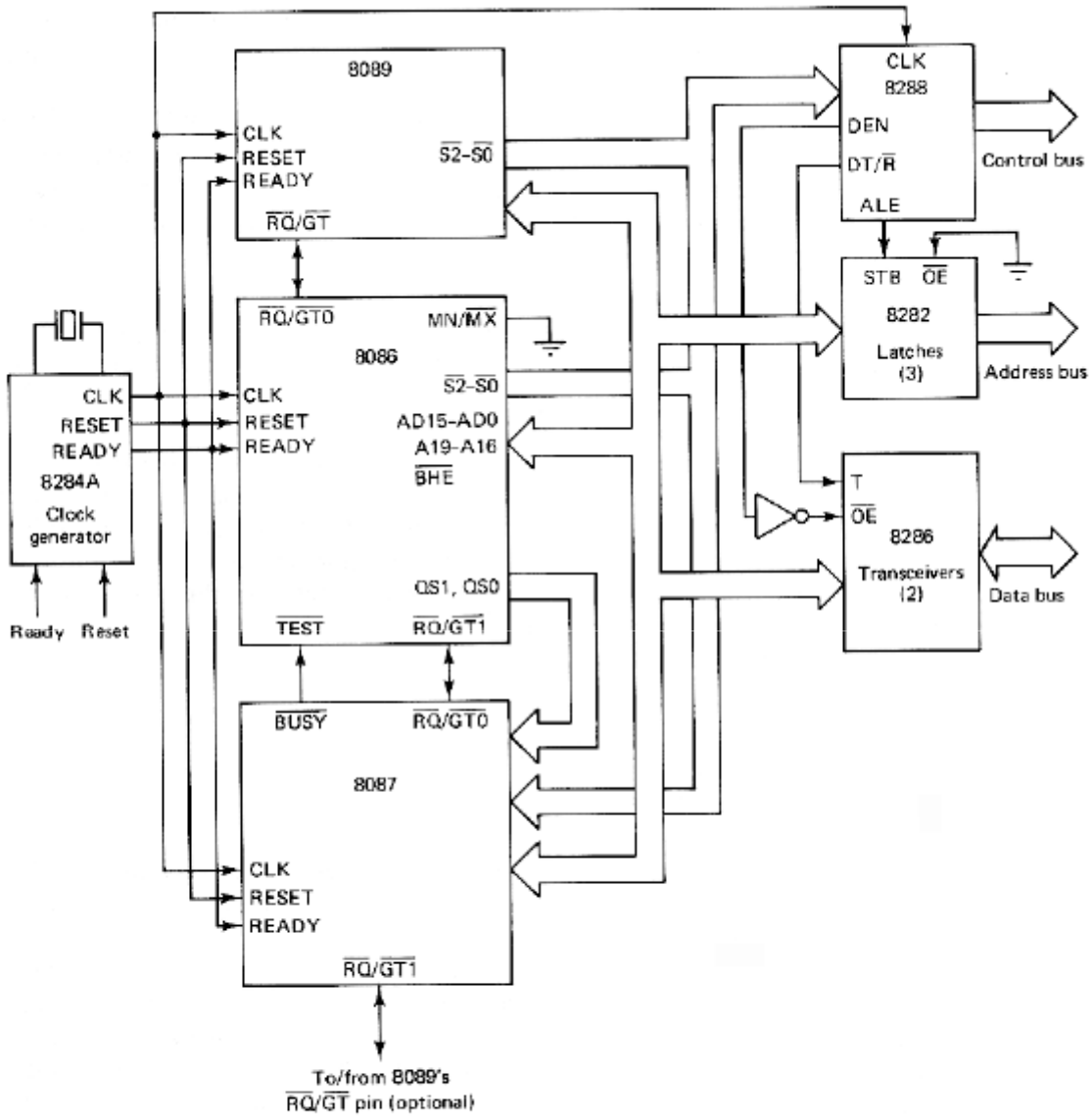
IOP Communication area

- SCPB(System Configuration pointer block)
  - It contains three words:
  - LS Byte specifies the width of system bus.
  - Two words store the offset and segment address of the location of the SCB.
- SCB
  - Offset and segment address of the beginning of two consecutive channel control blocks in the system space.
- CBs
  - CCW(channel Control word)
  - Busy(FF/00)
  - Parameter block's offset and segment address.

Three Forms of Commands

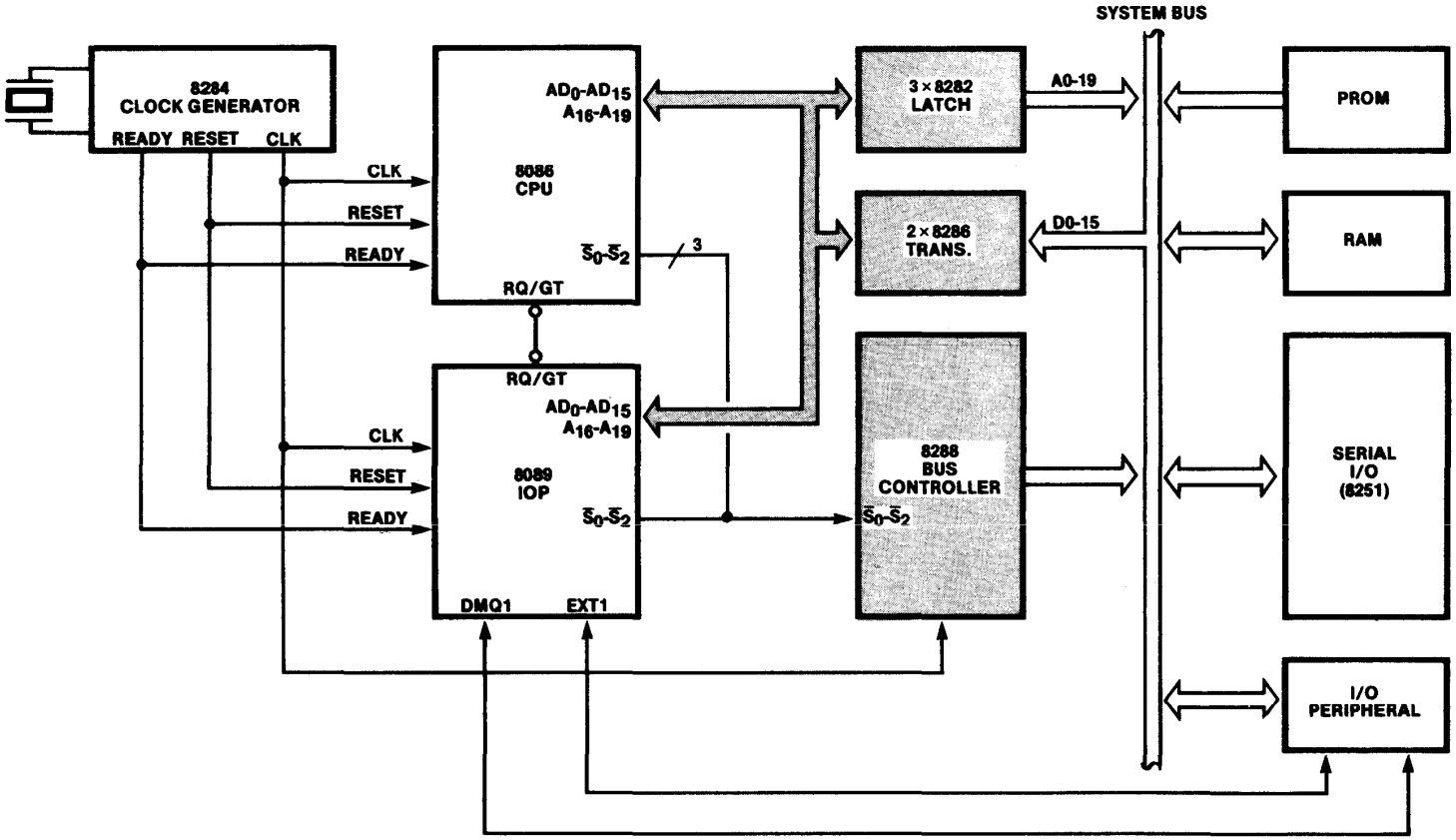
- Block transfer commands
  - Moves blocks data to IOP. Usually these instructions swap pages in and out of physical memory, and to load programs from disk memory.
- Arithmetic, logic, and Branch operations
  - IOP uses ALU instructions to manipulate the data so the process time for CPU is shorten.
- Control Command
  - Controls hardware.
    - Ex: rewind the tape on a tape drive or ejecting a CD from a drive.


8086/8088
Set up message
Wake up independent processor with OUT instruction
Execute 8086 instructions
Wait for ready or interrupt request
Independent Processor (8089)
Wait for request
Fetch the message
Perform requested task
Notify CPU of completion



NOTE: Interrupt system and other details are not shown.

Figure 11-8 Configuration involving both a coprocessor and an independent processor.


SYSTEM BUS
8284
CLOCK GENERATOR
READY RESET CLK
CLK
RESET
READY
8086
CPU
AD0-AD15
A16-A19
S0-S2
3
RQ/GT
RQ/GT
AD0-AD15
A16-A19
8089
IOP
S0-S2
DMQ1
EXT1
CLK
RESET
READY
3 x 8282
LATCH
A0-19
2 x 8286
TRANS.
D0-15
8288
BUS
CONTROLLER
S0-S2
PROM
RAM
SERIAL
I/O
(8251)
I/O
PERIPHERAL